UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/714,553	11/17/2000	Hiroyuki Suzuki	018656-190	5481

21839 7590 09/09/2004

BURNS DOANE SWECKER & MATHIS L L P
POST OFFICE BOX 1404
ALEXANDRIA, VA 22313-1404

EXAMINER	
DANG, DUY M	

ART UNIT	PAPER NUMBER
2621	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/714,553	SUZUKI ET AL.	
	Examiner	Art Unit	
	Duy M Dang	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 6/8/04.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 17 November 2000 is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment filed 6/8/04 has been entered and made of record.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 15 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Fukuchi (JP 11-317887. Art of recorded, IDS filed 3/27/01, paper #3. An English Translated copy is accompanied hereto).

Regarding claim 15, Fukuchi teaches:

a first circuit having a rewritable configuration (i.e., the "image processing circuit" shown at 11 in figure 2 having a Field Programmable Gate Array or FPGA according to abstract. This interpretation is consistent with applicant's disclosed page 6 lines 11-13)), and having a plurality of line memories (see "FIFO circuit" shown at 50 in figure 9 and 60 in figure 10. This interpretation is also consistent with applicant's disclosed page 7 line 2, page 9 lines 14 and 19);

a second circuit for processing image data output from the line memories (i.e., the "image processing circuit" shown at 11 of figure 2);

a memory for storing setting information for rewriting a configuration of the first circuit (see ROM 15 of figure 2 and mentioned in abstract, and further detailed in figure 4); and

a controller for rewriting a configuration of the line memories of the first circuit by use of the setting information stored in the memory based on an image processing condition (see CPU 14 of figure 2 and abstract, and the configurations of the FIFO shown in figures 9-10. These

configurations are used to reconfigure the memory FIFO to extend the memory capacity when required according to paragraphs 30-37).

Regarding claim 18, Fukuchi further teaches wherein the image processing condition is selectable from multiple values for a given output device (see table 1 shown in paragraph 17).

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-14 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuchi (JP 11-317887. Art of recorded, IDS filed 3/27/01, paper #3. An English Translated copy is accompanied hereto) in view of Dowling (US Patent No. 5,553,167).

Regarding claims 1 and 8, Fukuchi teaches an image processing apparatus (see "image processing unit" shown at 1 in figure 2 and mentioned in abstract) comprising:

a pixel matrix formation section (see "image processing circuit" shown at 11 in figure 2 and mentioned in abstract) having a rewritable circuit configuration (see "field programmable gate array FPGA" mentioned in abstract. This interpretation is consistent with applicant's disclosed page 6 lines 11-13), and having a plurality of line memories that output pixel data in parallel (see "FIFO circuit" shown at 50 in figure 9 and 60 in figure 10. This interpretation is also consistent with applicant's disclosed page 7 line 2, page 9 lines 14 and 19);

a memory for storing setting information for rewriting the circuit configurations of the pixel matrix formation section and the filtering circuit (see SDRAM (item 16) shown in figure 2 and ROM 15 shown in figure 4); and

a controller for rewriting a configuration of the line memories and the configuration of the filtering circuit by use of the setting information stored in the memory based on an image processing condition (see CPU 14 of figure 2 and abstract, and the configurations of the FIFO shown in figures 9-10. These configurations are used to reconfigure the memory FIFO to extend the memory capacity when required according to paragraphs 30-37).

Fukuchi fails to teaches "a filtering circuit consist of a device that has a rewritable configuration, and performing filtering of pixel data by use of a pixel matrix based on the pixel data received in parallel from the line memories". However, such features are well known in the art as evidenced by Dowling.

Dowling teaches a field programmable gate array or FPGA for performing as a filter circuit mentioned in column 10 lines 15-20. Using a filter would improve image quality. In addition, Applicant also uses FPGA as a filtering circuit as mentioned in specification page 7 line 13.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the FPGA as a filter as taught by Dowling in combination with Fukuchi in order to allow using FPGA as a filter thereby simplifying the system and enhancing heat reduction and cost saving, and improving image quality. This would also allow simple modification by using software/program when needed.

Regarding claims 2 and 9, Fukuchi further teaches output image size (see figure 7 and page 8 lines 29-32).

Regarding claims 3 and 10, both Fukuchi and Dowling fails to teaches wherein said image processing condition is a processing speed. However, it is well known in the art and

widely used in the commercial digital camera on the market (Official Notice) in order to allow a various choices to the user to where there is a limitation on storage capacity, and time is more priority than image quality.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the conventional features in combination with the combination of Fukuchi and Dowling for that reasons.

Regarding claims 4 and 11, Fukuchi further teaches an operation panel for setting the image processing condition (see "mode operation S4" of figure 5).

Regarding claims 5 and 12, Fukuchi further teaches wherein said controller rewrites the configuration of the processing circuit in accordance with the operation mode set with the operation panel (see flow chart shown in figure 5 and their corresponding text portion mentioned in page 7, 5 lines before last 13 lines).

Regarding claims 6 and 13, Dowling teaches wherein said filtering circuit is used for image area determination (see filter 200 of figure 2 and it corresponding text portion mentioned in col. 3 line 5 to col. 4 line 8. Specifically, Dowling teaches the use of detectors 208 (white detector) and 210 (black detector)).

Regarding claims 7 and 14, Dowling further teaches wherein the filtering circuit performs filtering for detecting an isolated point of an image (see the white detector 208 and black detector 210 included in filter 200 of figure 2 and further detailed in figures 3 and 5 for isolating the white pixel and black pixel. This interpretation appears to be consistent with Applicant's disclosed on page 8 lines 14-21).

Regarding claims 16-17, Fukuchi further teaches wherein the image processing condition is selectable from multiple values for a given output device (see table 1 shown in paragraph 17).

6. Applicant's arguments filed 6/8/04 have been fully considered but they are not persuasive.

A cited reference (US Patent No. 5,553,167) included in PTO-892 is attached herein in response to Applicant's remarks stated in second paragraph of page 7.

Applicant's amendment and remarks stated in paragraph 3 of page 7 overcome claim rejection under section 35 USC 112, 2nd paragraph.

In reply to Applicant's remarks with regard to claim 15, see page 8 to line 7 of page 10, that Fukuchi does not teach reconfiguring memory, the examiner disagrees and reasons as follows: In Fukuchi, the memory FIFO is reconfigured to extend the memory capacity when required according to paragraphs 30-37.

In reply to Applicant's remarks with regard to claims 1 and 8 (page 10 line 11 to page 13 line 3) that the Fukuchi and Dowling references can not be combined. Applicant is reminded that, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, both Fukuchi and Dowling teach the same field of invention that of image processing, and the use of a Field Programmable Gate Array (FPGA). Dowling suggests to use a FPGA as a filter in column 10 lines 15-20 (Note that this is similar to Applicant's disclosed on

page 7 lines 1-3 of the specification) and its advantages mentioned in column 1 lines 41-50. Therefore, the combination of Fukuchi and Dowling are proper.

In reply to Applicant's remarks with regard to claims 3 and 11, see 1st full paragraph of page 13. It is noted that Applicant has challenged to the Examiner's Official Notice taken in the previous office action for these claimed features. It is also noted that Applicant has failed to state why the notice fact is not considered to be common knowledge or well-known in the art. Therefore, Applicant's remark is considered inadequately. See 37 CFR 1.104(d)(2).

In reply to Applicant's remarks with regard to claims 4-5 and 11-12 that Fukuchi does not teach operation panel (last paragraph of page 13 to line 5 of page 14). Applicant is reminded that the examiner is entitled to give the broadest reasonable interpretation to the language of the claims. So the examiner considers Fukuchi's operation mode S4 shown in figure 5 to be Applicant's operation panel within the broad meaning of the term. The examiner is not limited to applicant's definition which is not specifically set forth in the claims. *In re Tanaka et al., 193 USPQ, (CCPA) 1977.*

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

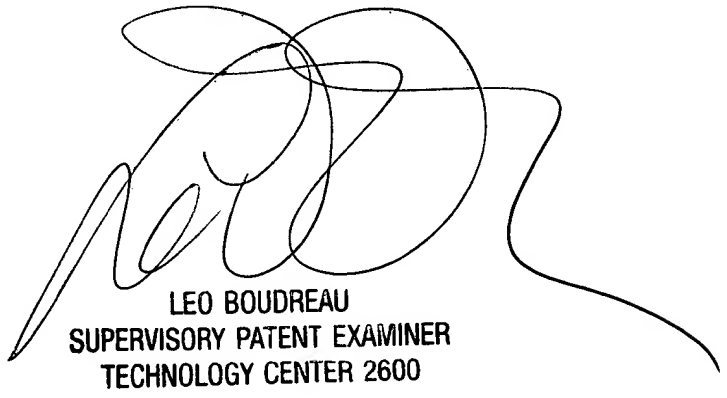
however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duy M Dang whose telephone number is 703-305-1464. The examiner can normally be reached on Monday to Thursday from 6:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo H Boudreau can be reached on 703-305-4706. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-0377.

dmd
9/3/04



LEO BOUDREAU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600